Fig. 1

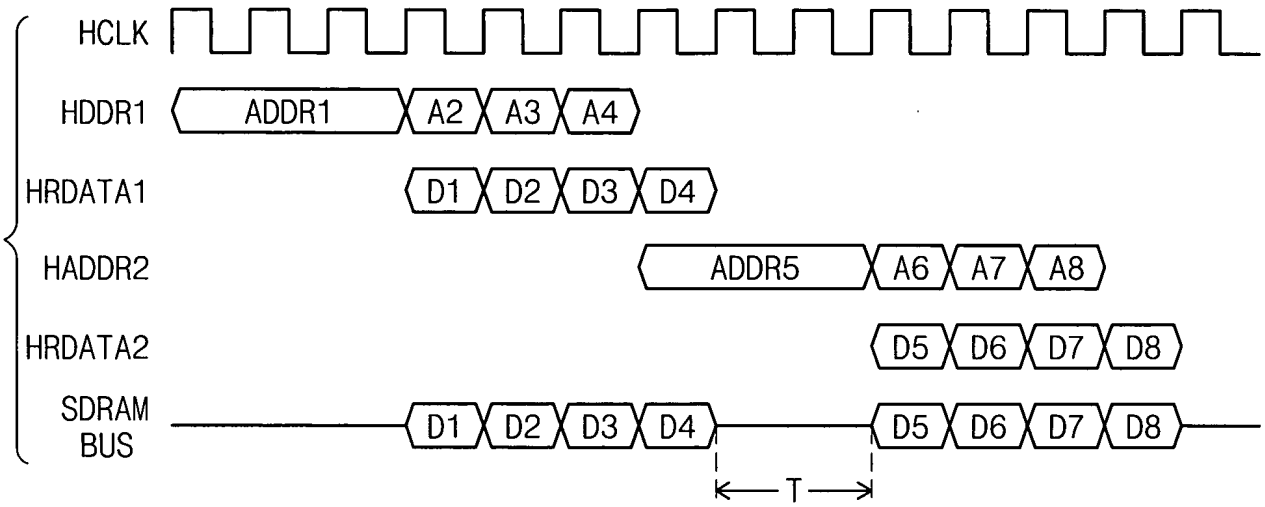

HCLK
HDDR1
ADDR1
A2
A3
A4
HRDATA1
D1
D2
D3
D4
HADDR2
ADDR5
A6
A7
A8
HRDATA2
D5
D6
D7
D8
SDRAM BUS
D1
D2
D3
D4
D5
D6
D7
D8
T

Fig. 2

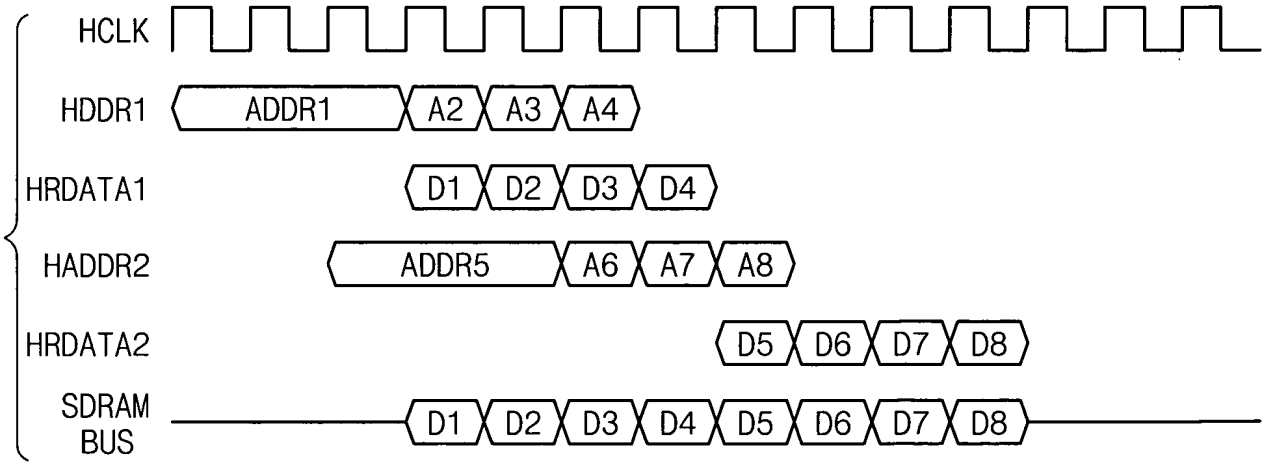

HCLK
HDDR1
ADDR1
A2
A3
A4
HRDATA1
D1
D2
D3
D4
HADDR2
ADDR5
A6
A7
A8
HRDATA2
D5
D6
D7
D8
SDRAM BUS
D1
D2
D3
D4
D5
D6
D7
D8

Fig. 3

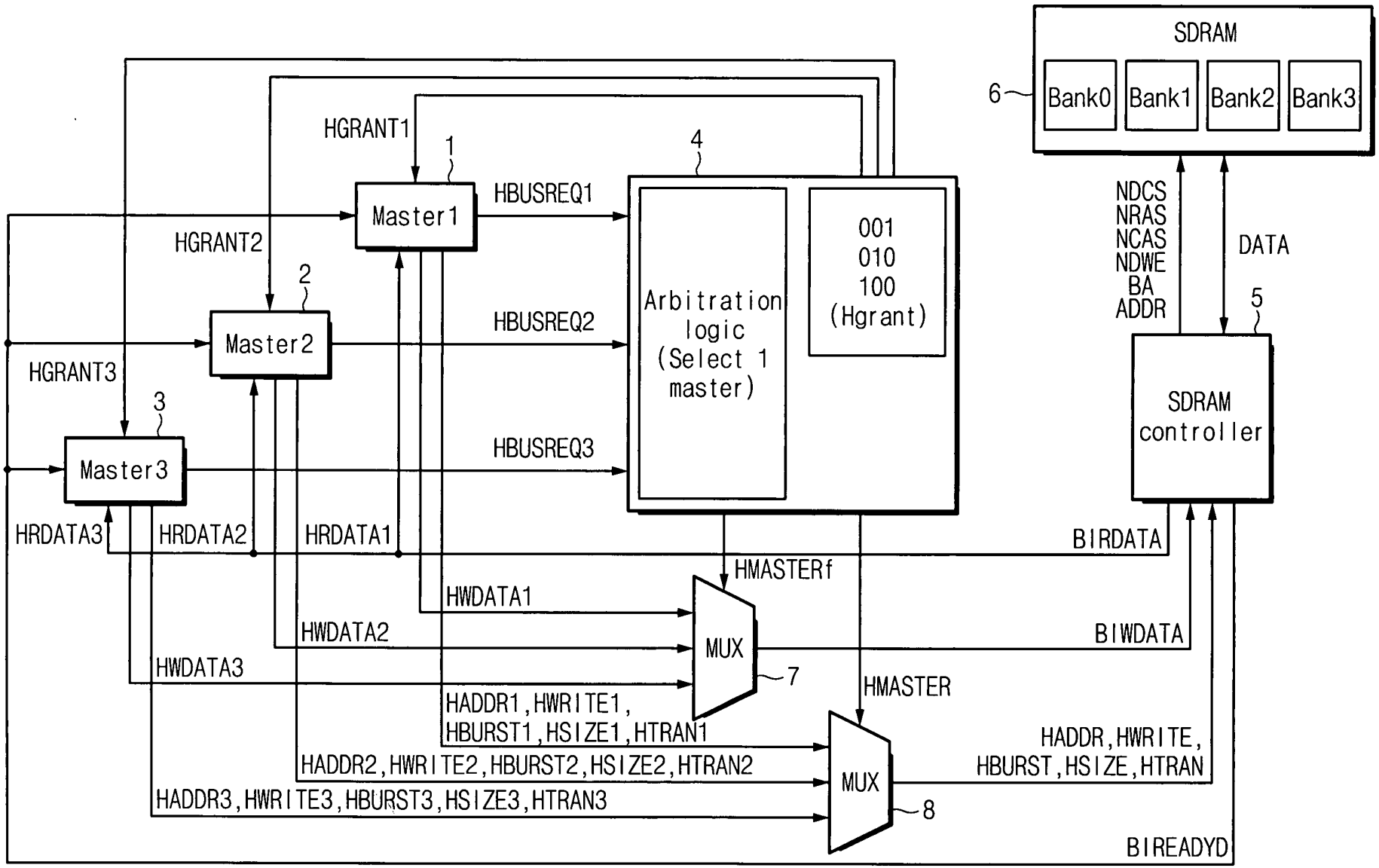

SDRAM
6
Bank0
Bank1
Bank2
Bank3
HGRANT1
1
4
Master1
HBUSREQ1
HGRANT2
2
Master2
HBUSREQ2
HGRANT3
3
Master3
HBUSREQ3
Arbitration logic (Select 1 master)
001
010
100
(Hgrant)
NDCS
NRAS
NCAS
NDWE
BA
ADDR
DATA
5
SDRAM controller
HRDATA3
HRDATA2
HRDATA1
BIRDATA
HMASTERf
HWDATA1
HWDATA2
HWDATA3
MUX
7
BIWDATA
HMASTER
HADDR1, HWRITE1, HBURST1, HSIZE1, HTRAN1
HADDR2, HWRITE2, HBURST2, HSIZE2, HTRAN2
HADDR3, HWRITE3, HBURST3, HSIZE3, HTRAN3
MUX
8
HADDR, HWRITE, HBURST, HSIZE, HTRAN
BIREADYD

Fig. 4

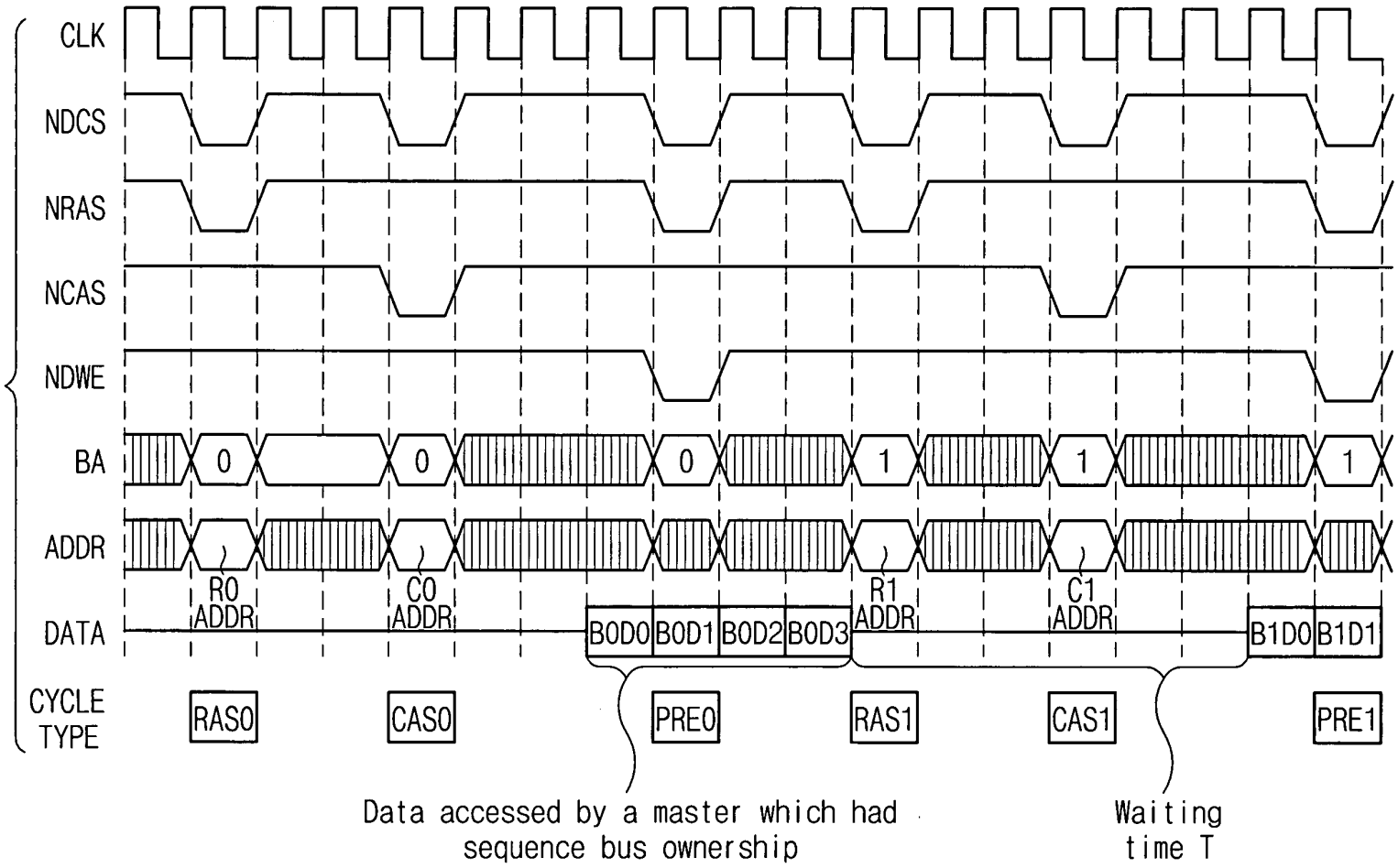

CLK
NDCS
NRAS
NCAS
NDWE
BA
ADDR
DATA
CYCLE TYPE
0
0
0
1
1
1
R0 ADDR
C0 ADDR
R1 ADDR
C1 ADDR
B0D0
B0D1
B0D2
B0D3
B1D0
B1D1
RAS0
CAS0
PRE0
RAS1
CAS1
PRE1
Data accessed by a master which had sequence bus ownership
Waiting time T

Fig. 5

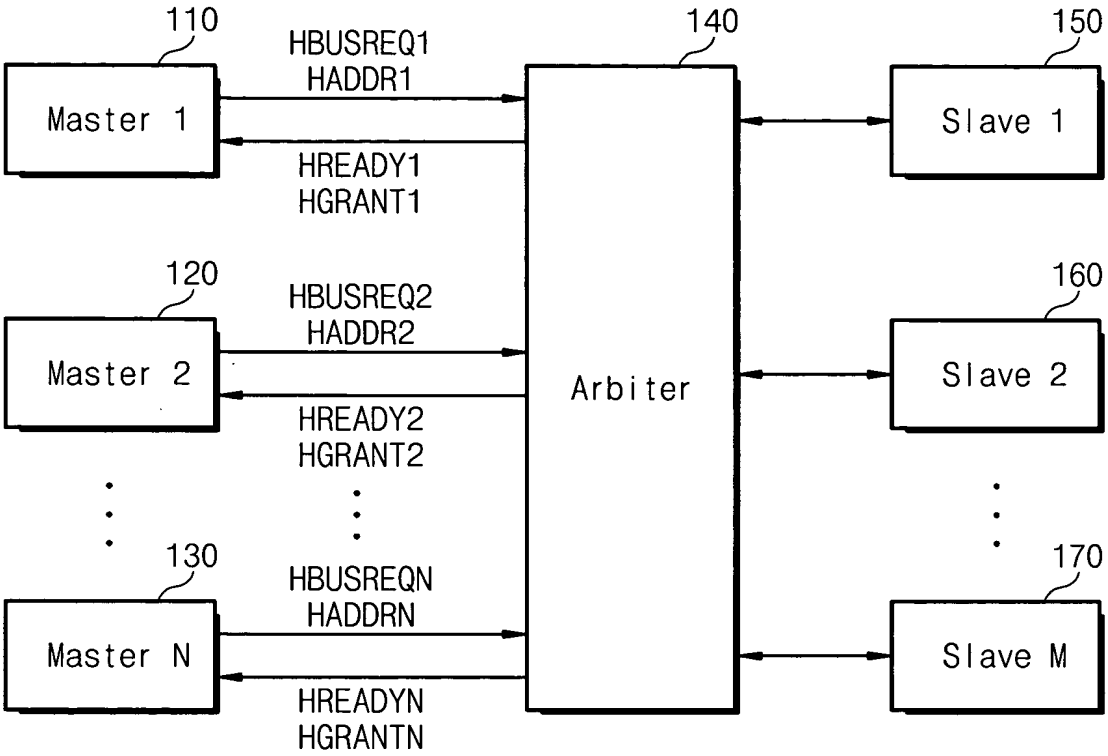

110
Master 1
HBUSREQ1
HADDR1
HREADY1
HGRANT1
120
Master 2
HBUSREQ2
HADDR2
HREADY2
HGRANT2
130
Master N
HBUSREQN
HADDRN
HREADYN
HGRANTN
140
Arbiter
150
Slave 1
160
Slave 2
170
Slave M

Fig. 6

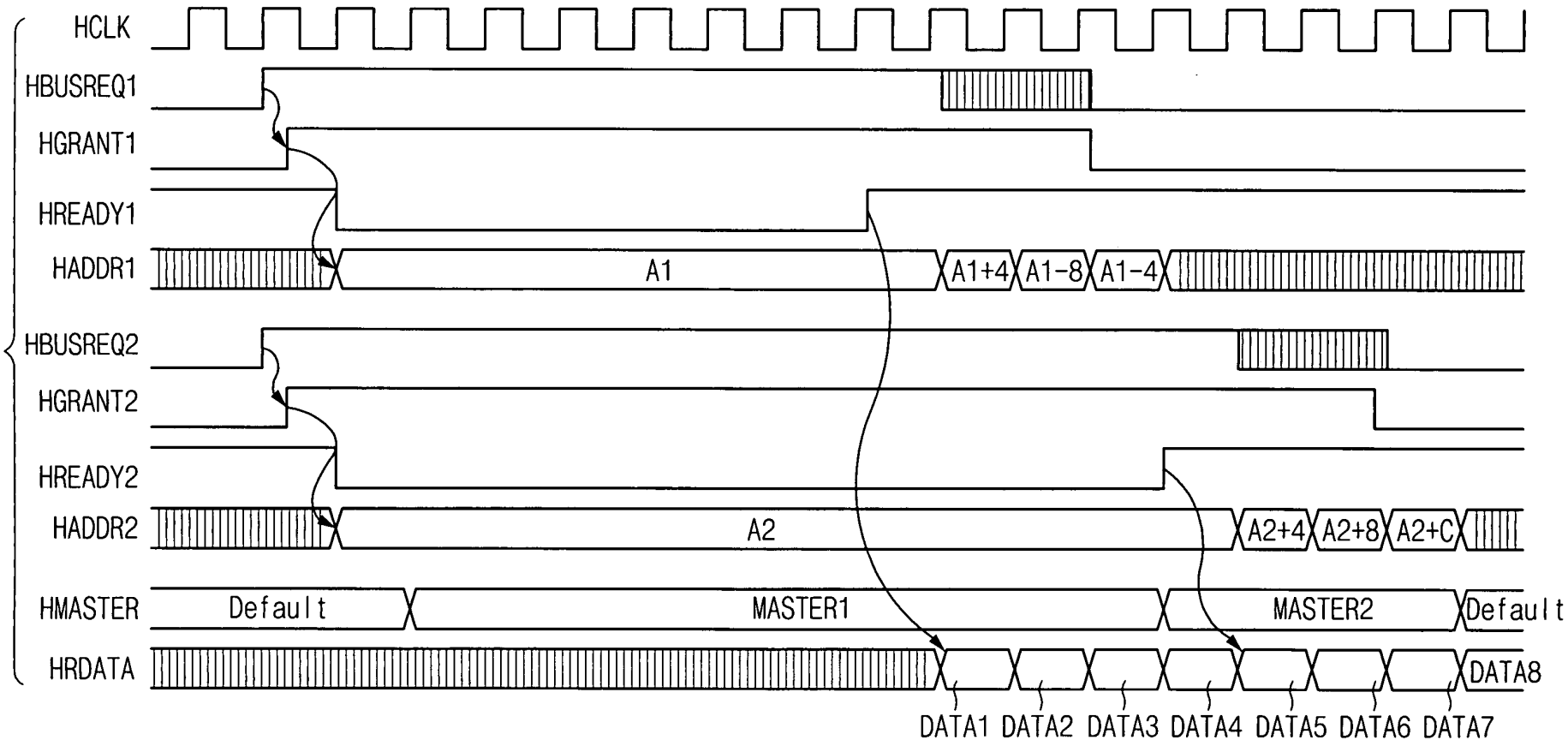

HCLK
HBUSREQ1
HGRANT1
HREADY1
HADDR1
A1
A1+4
A1-8
A1-4
HBUSREQ2
HGRANT2
HREADY2
HADDR2
A2
A2+4
A2+8
A2+C
HMASTER
Default
MASTER1
MASTER2
Default
HRDATA
DATA8
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7

Fig. 7

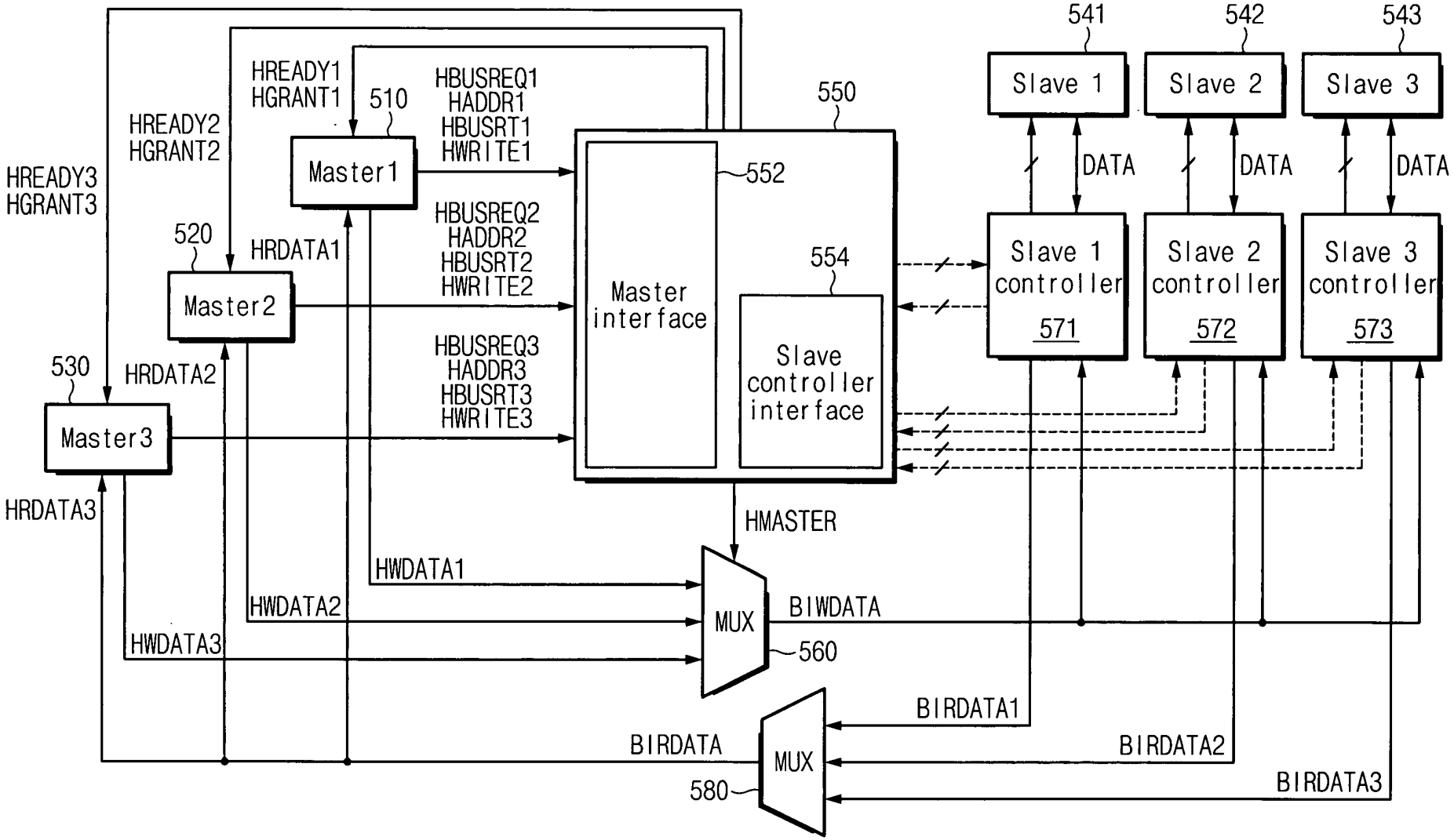

HREADY1
HGRANT1
510
HBUSREQ1
HADDR1
HBUSRT1
HWRITE1
HREADY2
HGRANT2
HREADY3
HGRANT3
Master1
550
552
HBUSREQ2
HADDR2
HBUSRT2
HWRITE2
520
HRDATA1
Master2
554
Master interface
Slave controller interface
HBUSREQ3
HADDR3
HBUSRT3
HWRITE3
530
HRDATA2
Master3
HRDATA3
HMASTER
HWDATA1
HWDATA2
HWDATA3
MUX
560
BIWDATA
BIRDATA
MUX
580
BIRDATA1
BIRDATA2
BIRDATA3
541
542
543
Slave 1
Slave 2
Slave 3
DATA
DATA
DATA
Slave 1 controller 571
Slave 2 controller 572
Slave 3 controller 573

Fig. 8

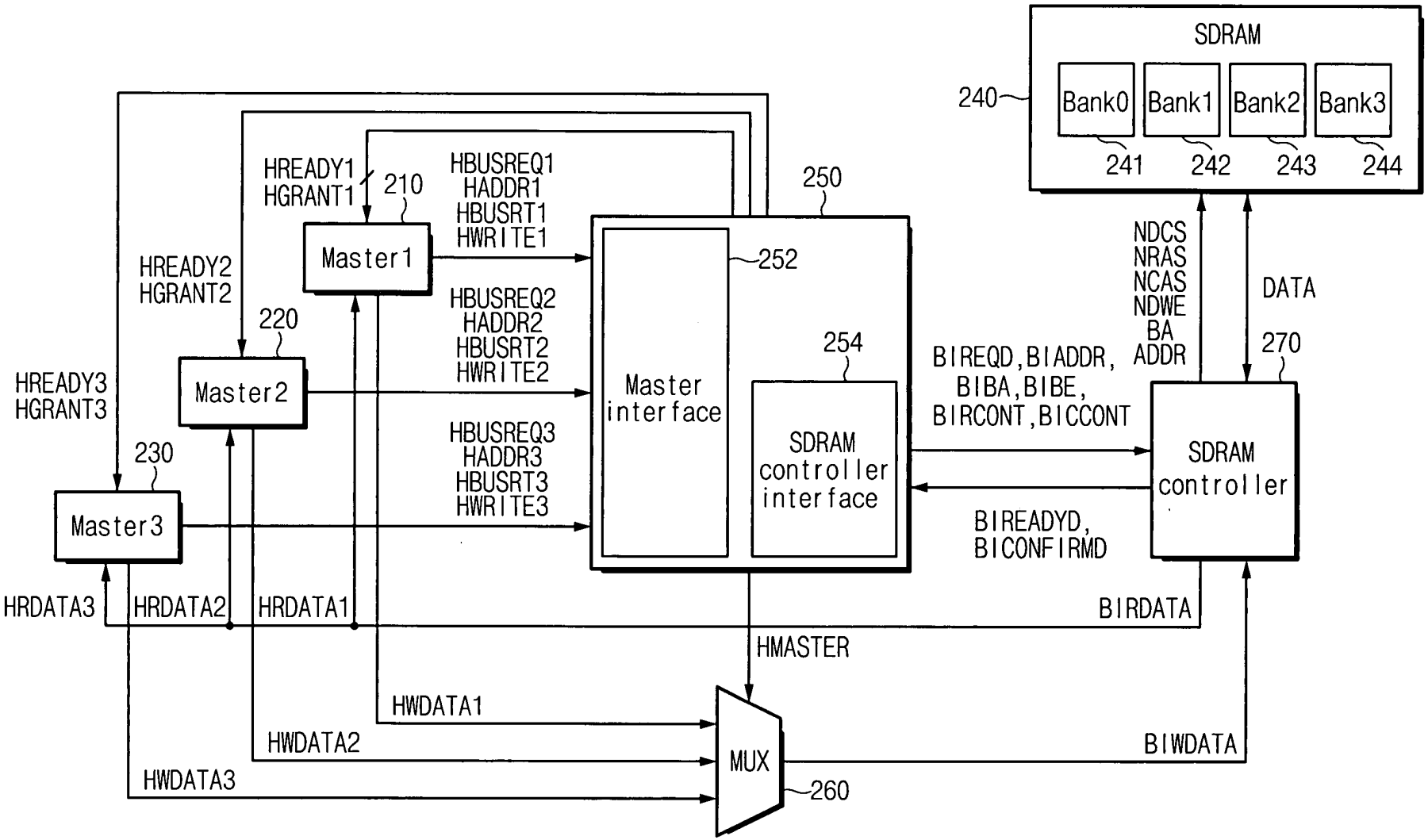

SDRAM
240
Bank0
Bank1
Bank2
Bank3
241
242
243
244
250
252
254
210
220
230
270
Master1
Master2
Master3
Master interface
SDRAM controller interface
SDRAM controller
HREADY1
HGRANT1
HREADY2
HGRANT2
HREADY3
HGRANT3
HBUSREQ1
HADDR1
HBUSRT1
HWRITE1
HBUSREQ2
HADDR2
HBUSRT2
HWRITE2
HBUSREQ3
HADDR3
HBUSRT3
HWRITE3
NDCS
NRAS
NCAS
NDWE
BA
ADDR
DATA
BIREQD, BIADDR,
BIBA, BIBE,
BIRCONT, BICCONT
BIREADYD,
BICONFIRMD
BIRDATA
HRDATA3
HRDATA2
HRDATA1
HMASTER
HWDATA1
HWDATA2
HWDATA3
MUX
260
BIWDATA

Fig. 9

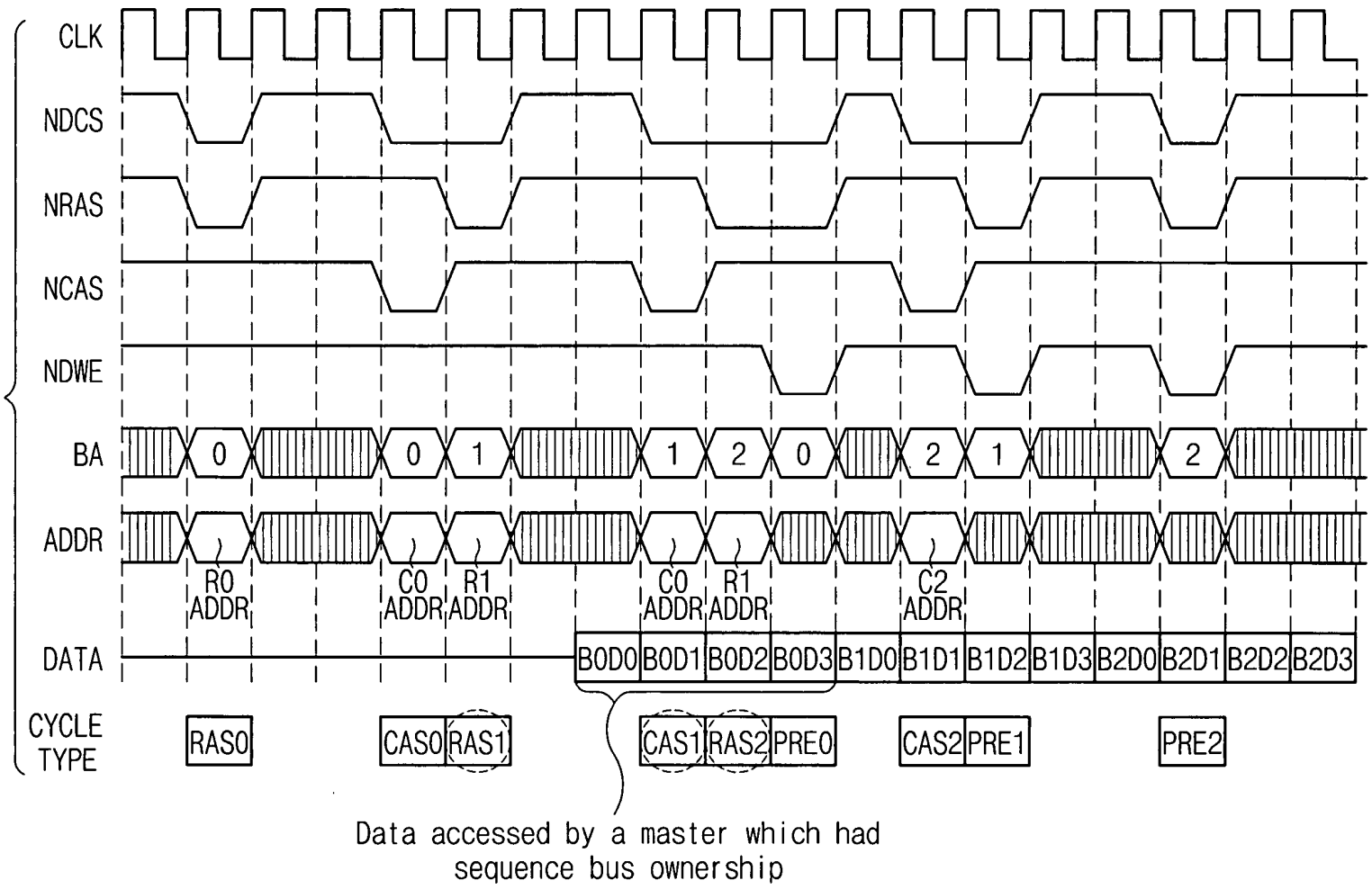

CLK
NDCS
NRAS
NCAS
NDWE
BA
0
0
1
1
2
0
2
1
2
ADDR
R0 ADDR
C0 ADDR
R1 ADDR
C0 ADDR
R1 ADDR
C2 ADDR
DATA
B0D0
B0D1
B0D2
B0D3
B1D0
B1D1
B1D2
B1D3
B2D0
B2D1
B2D2
B2D3
CYCLE TYPE
RAS0
CAS0
RAS1
CAS1
RAS2
PRE0
CAS2
PRE1
PRE2
Data accessed by a master which had sequence bus ownership

Fig. 10

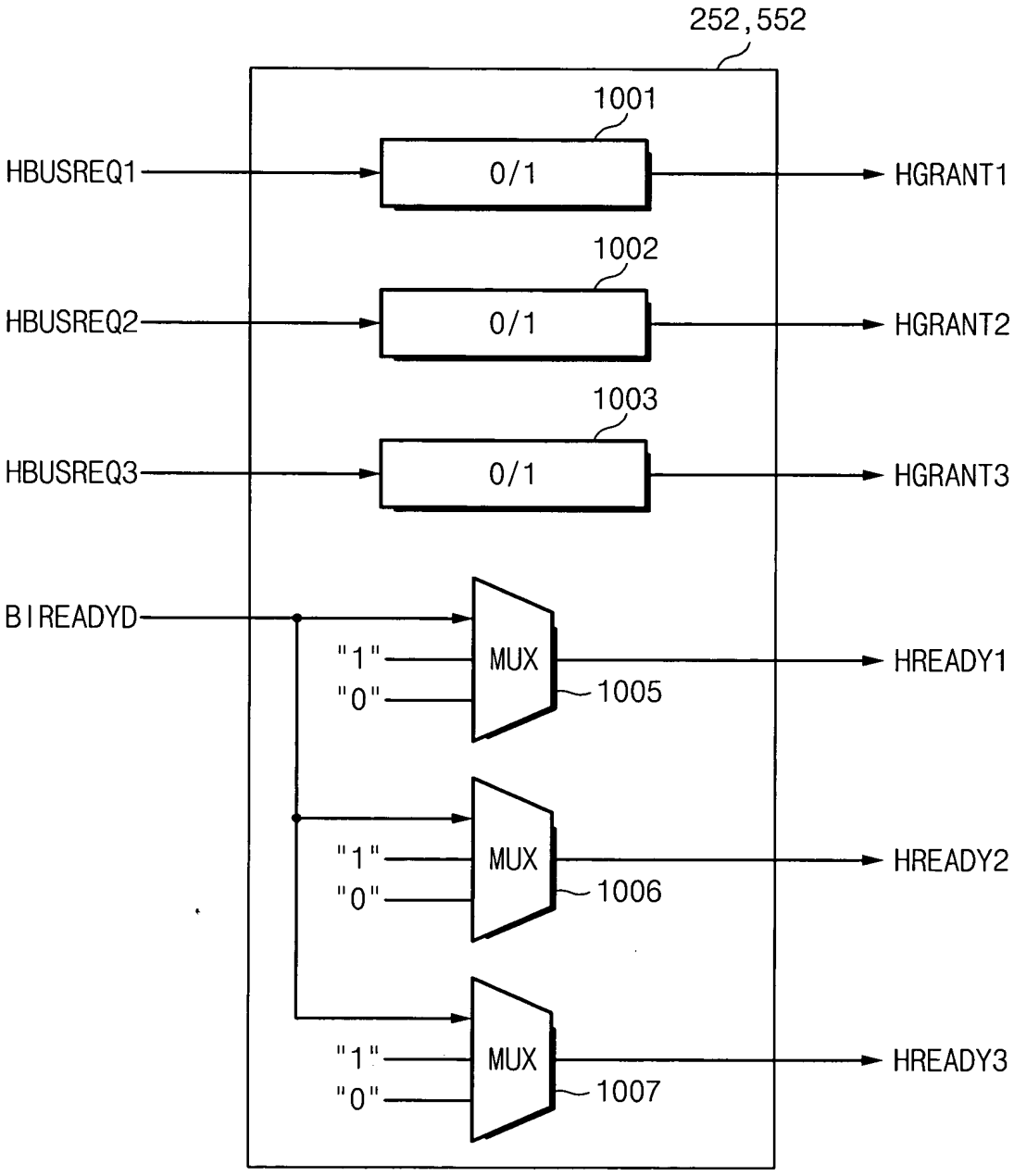

252,552
1001
HBUSREQ1
0/1
HGRANT1
1002
HBUSREQ2
0/1
HGRANT2
1003
HBUSREQ3
0/1
HGRANT3
BIREADYD
"1"
"0"
MUX
1005
HREADY1
"1"
"0"
MUX
1006
HREADY2
"1"
"0"
MUX
1007
HREADY3

Fig. 11

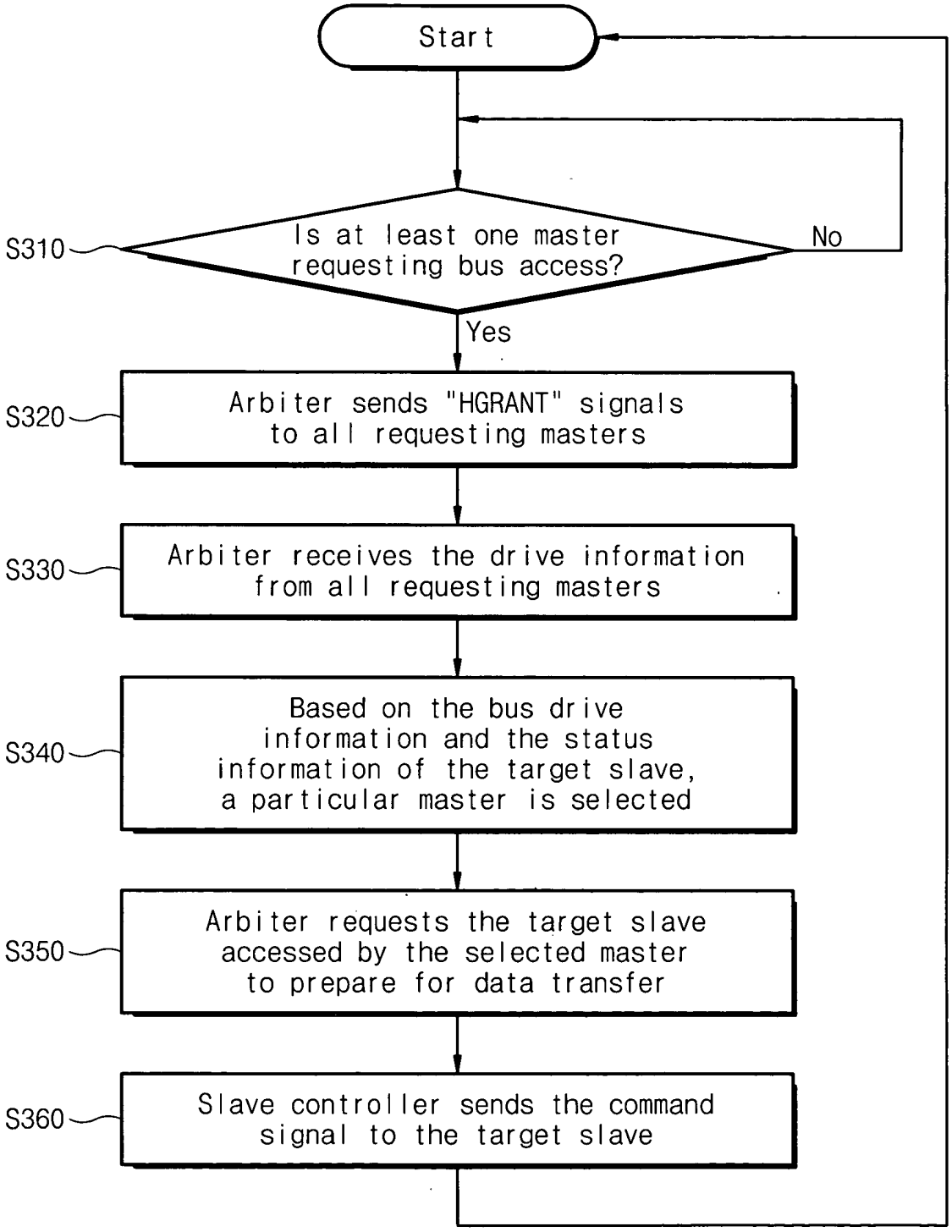
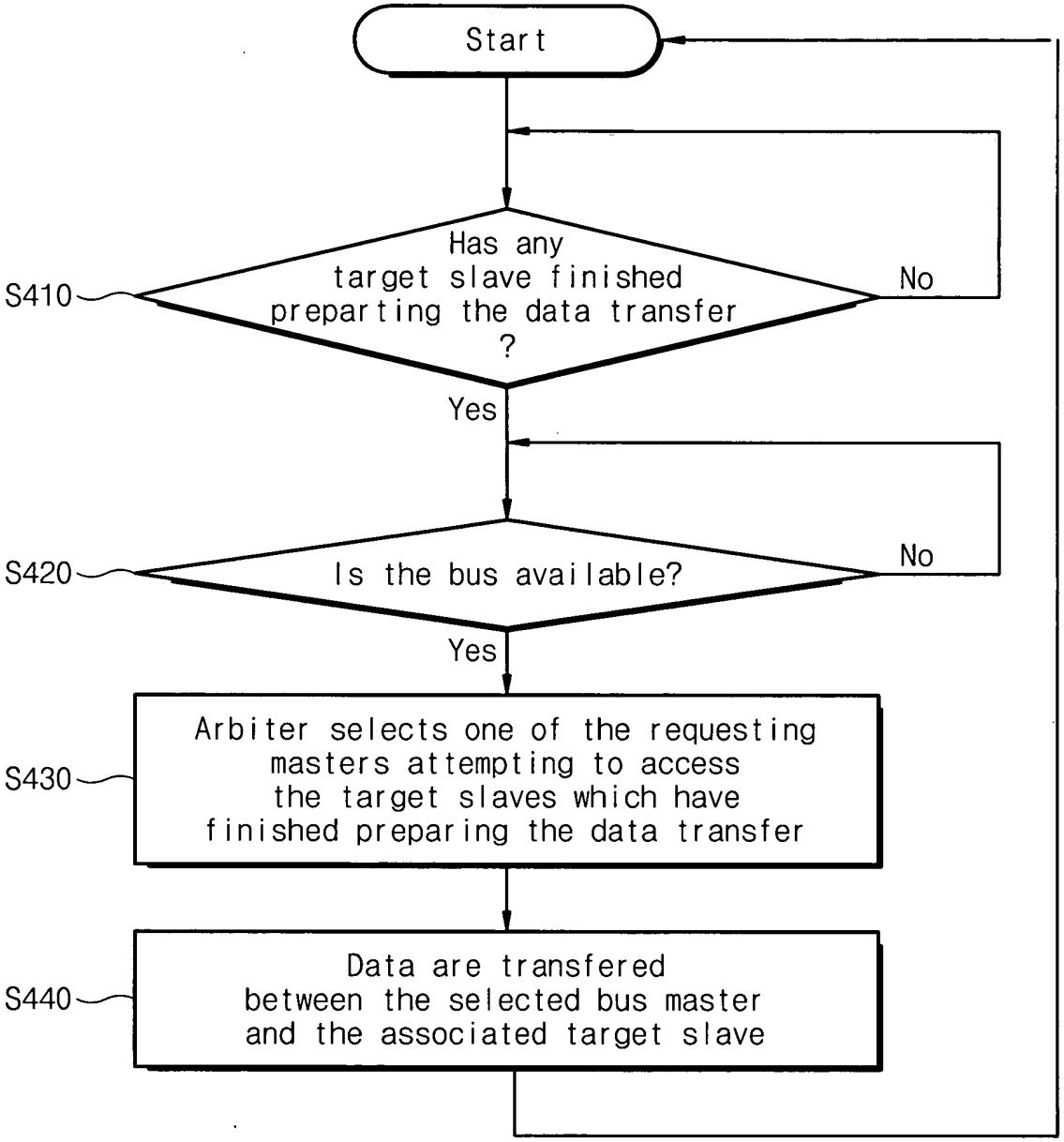

Start
S310
Is at least one master requesting bus access?
No
Yes
S320
Arbiter sends "HGRANT" signals to all requesting masters
S330
Arbiter receives the drive information from all requesting masters
S340
Based on the bus drive information and the status information of the target slave, a particular master is selected
S350
Arbiter requests the target slave accessed by the selected master to prepare for data transfer
S360
Slave controller sends the command signal to the target slave

Fig. 12


Start
S410
Has any target slave finished preparting the data transfer ?
No
Yes
S420
Is the bus available?
No
Yes
S430
Arbiter selects one of the requesting masters attempting to access the target slaves which have finished preparing the data transfer
S440
Data are transfered between the selected bus master and the associated target slave